1. A split gate flash memory cell structure for prevention of reverse tunneling comprising:

a semiconductor region within a substrate extending to a surface;

a gate insulator layer formed over said semiconductor surface;

a conductive floating gate disposed over said gate insulator layer

a floating gate insulator layer disposed over said floating gate and sidewall insulator spacers disposed along bottom portion of sidewalls of said floating gate adjacent to said gate insulator layer, where etching processes used to fashion said sidewall insulator spacers from a spacer insulator layer, etch said spacer insulator layer faster than said gate insulator layer and said floating gate insulator layer;

an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate , said floating gate insulator layer and said sidewall insulator spacers;

a conductive control gate disposed over said intergate insulator layer and covering about half of said floating gate.

2. The structure of Claim 1 wherein said semiconductor region is a silicon region.

3. The structure of Claim 1 wherein said substrate is a silicon containing substrate.

4. The structure of Claim 1 wherein said gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms.

5. The structure of Claim 1 wherein said conductive floating gate is composed of polysilicon.

6. The structure of Claim 1 wherein said floating gate insulator layer is a grown polysilicon oxide layer grown to a thickness of about 800 to 2000 Angstroms.

7. The structure of Claim 1 wherein said spacer insulator layer is an oxide layer.

8. The structure of Claim 1 wherein said spacer insulator layer is a PECVD oxide layer.

9. The structure of Claim 1 wherein said spacer insulator layer is a deposited oxide layer, said gate insulator layer is a thermal oxide layer and said floating gate insulator layer is a polysilicon oxide layer.

10. The structure of Claim 1 wherein said etching processes used to fashion said sidewall insulator spacers from said spacer insulator layer are an anisotropic dry etch leaving some of said spacer insulator layer everywhere followed by a wet etch leaving only said sidewall insulator spacers.

11. The structure of Claim 1 wherein said intergate insulator layer is an oxide layer.

12. The structure of Claim 1 wherein said conductive control gate is composed of polysilicon.

13. A method for forming a split gate flash memory cell that prevents reverse tunneling comprising:

providing a semiconductor region within a substrate extending to a surface;

forming a gate insulator layer over said semiconductor surface;

forming a conductive floating gate disposed over said gate insulator layer with a floating gate insulator layer disposed over said floating gate;

depositing a spacer insulator layer over exposed portions of said gate insulator layer, said floating gate and said floating gate insulator layer;

etching said spacer insulator layer to fashion sidewall insulator spacers along bottom portion of said floating gate sidewall adjacent to said gate insulator layer;

forming an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate , said floating gate insulator layer and said sidewall insulator spacers;

forming a conductive control gate disposed over said intergate insulator layer and covering about half of said floating gate.

14. The method of Claim 13 wherein said semiconductor region is a silicon region.

15. The method of Claim 13 wherein said substrate is a silicon containing substrate.

16. The method of Claim 13 wherein said gate insulator layer is a thermally grown oxide layer.

17. The method of Claim 13 wherein said conductive floating gate is composed of polysilicon.

18. The method of Claim 13 wherein said floating gate insulator layer is a thermally grown polysilicon oxide layer.

19. The method of Claim 13 wherein said floating gates and floating gate insulator layer are formed by depositing a polysilicon layer over said gate insulator layer, depositing a hard mask layer over said polysilicon layer, patterning and etching said hard mask to expose a floating gate pattern on said polysilicon layer, growing a thermal polysilicon oxide over said exposed polysilicon layer to form said floating gate insulator layer, removing remaining said hard mask layer and etching said polysilicon layer stopping at said gate insulator layer.

20. The method of Claim 13 wherein said floating gates and floating gate insulator layer are formed by depositing a polysilicon layer over said gate insulator layer, depositing a hard mask layer over said polysilicon layer, patterning and etching said hard mask to expose a floating gate pattern on said polysilicon layer, growing a thermal polysilicon oxide over said exposed polysilicon layer to form said floating gate insulator layer, removing remaining said hard mask layer and etching said polysilicon layer stopping at said gate insulator layer and wherein said hard mask layer is a nitride layer.

21. The method of Claim 13 wherein said floating gates and floating gate insulator layer are formed by depositing a polysilicon layer over said gate insulator layer, depositing a hard mask layer over said polysilicon layer, patterning and etching said hard mask to expose a floating gate pattern on said polysilicon layer, growing a thermal polysilicon oxide over said exposed polysilicon layer to form said floating gate insulator layer, removing remaining said hard mask layer and etching said polysilicon layer stopping at said gate insulator layer and wherein said patterning and etching of said hard mask layer is accomplished by forming a photoresist layer, patterning said photoresist layer and etching said hard mask layer stopping at the said polysilicon layer and removing said photoresist layer.

22. The method of Claim 13 wherein said floating gates and floating gate insulator layer are formed by depositing a polysilicon layer over said gate insulator layer, depositing a hard mask layer over said polysilicon layer, patterning and etching said hard mask to expose a floating gate pattern on said polysilicon layer, growing a thermal polysilicon oxide over said exposed polysilicon layer to form said floating gate insulator layer, removing remaining said hard mask layer and etching said polysilicon layer stopping at said gate insulator layer and wherein said growing of said thermal polysilicon oxide is performed at about 800^0C - 1150^0C to a thickness of about 500-3000 Angstroms.

23. The method of Claim 13 wherein said spacer insulator layer is an oxide layer.

24. The method of Claim 13 wherein said spacer insulator layer is a deposited oxide layer, said gate insulator layer is a thermal oxide layer and said floating gate insulator layer is a polysilicon oxide layer.

25. The method of Claim 13 wherein said etching processes used to fashion said sidewall insulator spacers from said spacer insulator layer are an anisotropic dry etch leaving some of said

spacer insulator layer everywhere followed by a wet etch leaving only said sidewall insulator spacers layer.

26. The method of Claim 13 wherein said intergate insulator layer is an oxide layer.

27. The structure of Claim 13 wherein said conductive control gate is composed of polysilicon.